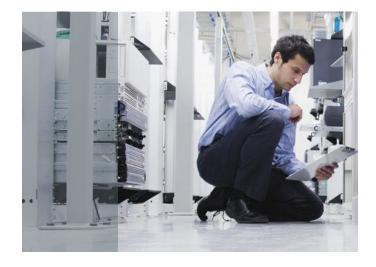
Introduction to Jitter Techniques for High Speed Serial Technologies

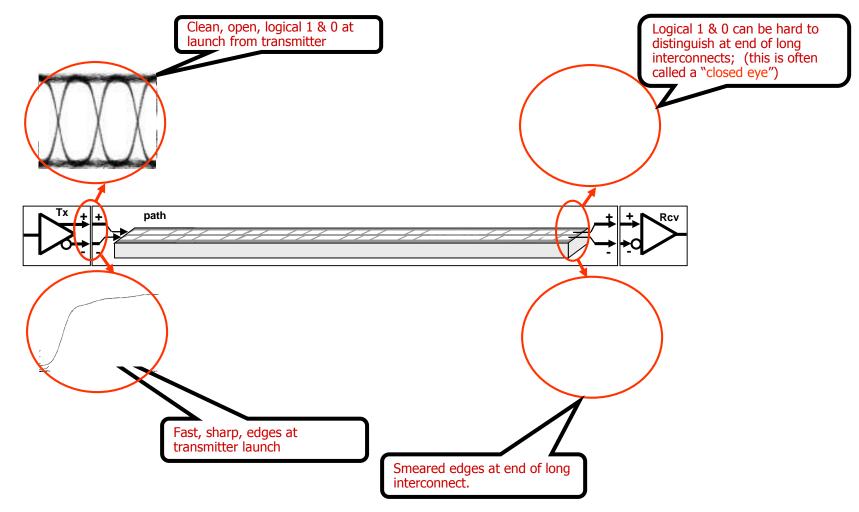






Industry Trends

Fast Data Rates, More HF Loss

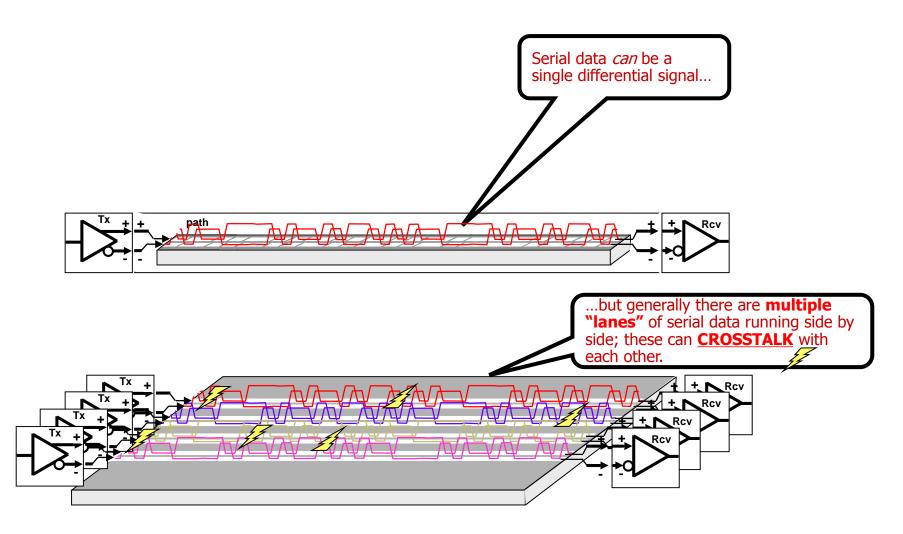


Reference Maxim Note HFDN-27.0 (Rev. 0, 09/03)



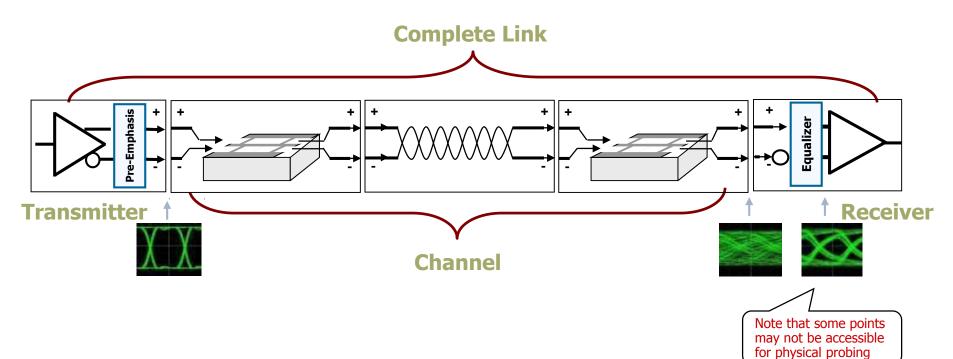
Industry Trends

Multiple Lanes Result in Crosstalk



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Anatomy of a Serial Data Link



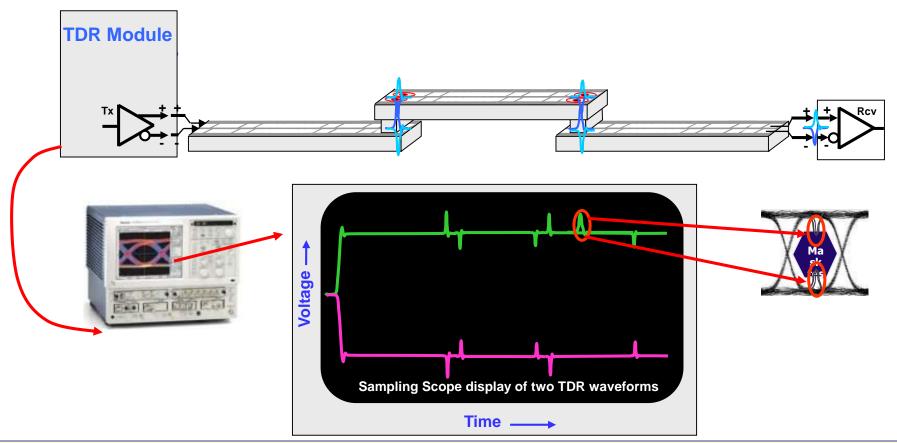
Aspirational goal: 0 errors Practical Goal: Bit Error Rate < Target BER

• Since BER is the ultimate goal, why not measure it directly?

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TDR Measurements Basics

TDR Basics



Transition points involve combinations of solder joints, circuit board vias, and connectors:

these all can have substantial effect on the total link performance.

TDR also is capable of producing **S-parameters**



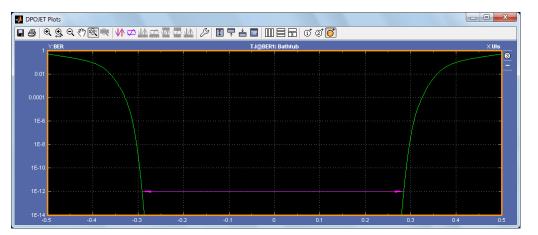
Jitter Basics

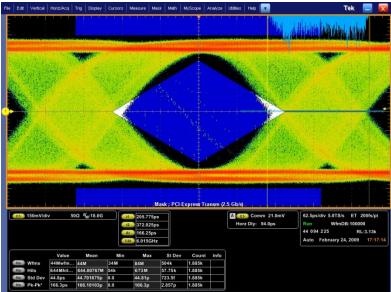
Definitions

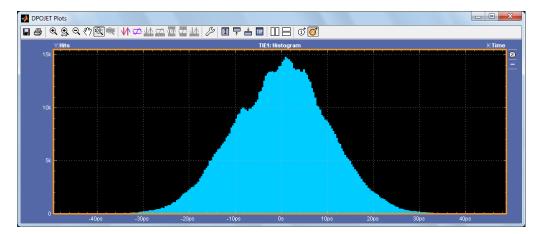




Jitter Plot?



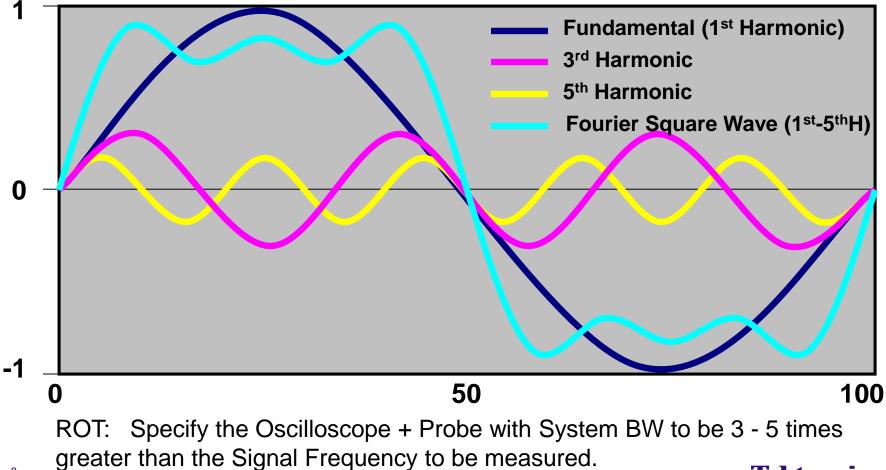






Bandwidth & Harmonics

Digital Square Wave – Odd Fourier Sums

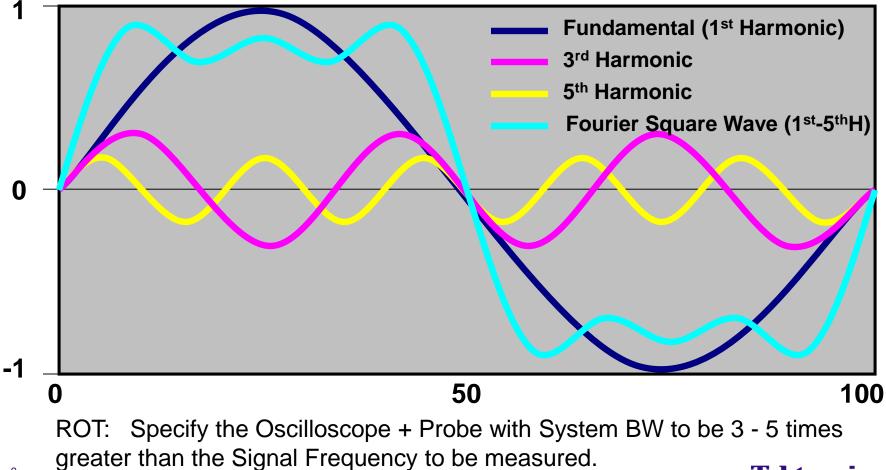


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Bandwidth & Harmonics

Digital Square Wave – Odd Fourier Sums

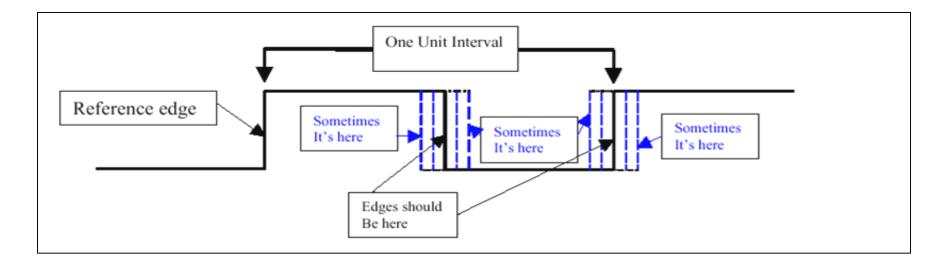


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What is Jitter?

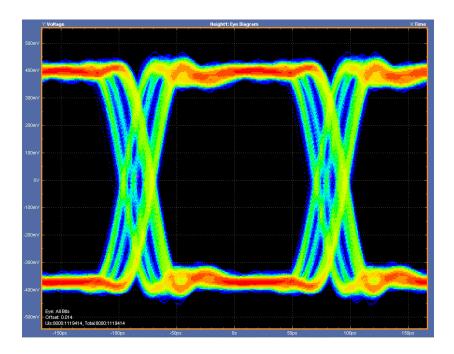
- Definitions
 - "The deviation of an edge from where it should be"
 - ITU Definition of Jitter: "Short-term variations of the significant instants of a digital signal from their ideal positions in time"





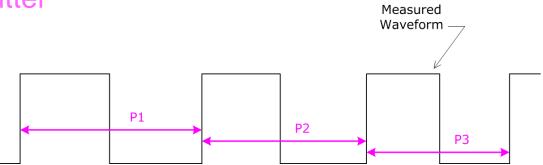
Jitter is caused by many things...

- Causes of Random Jitter
 - Thermal noise
 - Generally Gaussian
 - External radiation sources
 - Like background conversations...random and ever changing
- Causes of Periodic Jitter
 - Injected noise (EMI/RFI) & Circuit instabilities
 - Usually a fixed and identifiable source like power supply and oscillators
 - Will often have harmonic content
 - Transients on adjacent traces
 - Cabling or wiring (crosstalk)
 - PLL's problems
 - Loop bandwidth (tracking & overshoot)
 - Deadband (oscillation / hunting)
- Causes of Data Dependent Jitter
 - Transmission Losses
 - There is no such thing as a perfect conductor
 - Circuit Bandwidth
 - Skin Effect Losses
 - Dielectric Absorption
 - Dispersion esp. Optical Fiber
 - Reflections, Impedance mismatch, Path discontinuities (connectors)



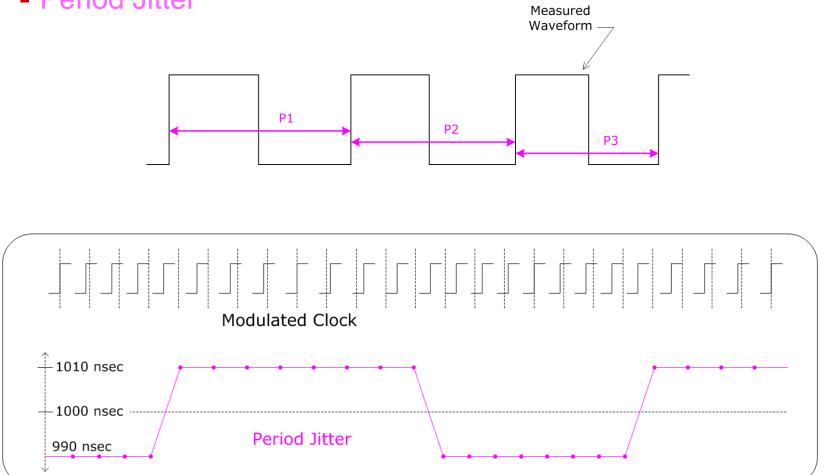


Period Jitter



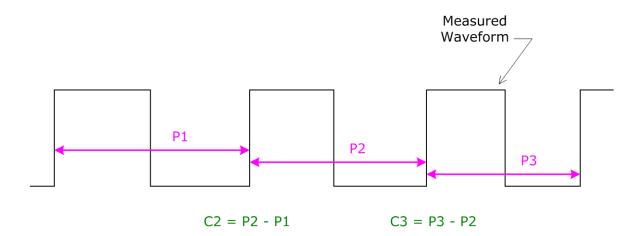


Period Jitter





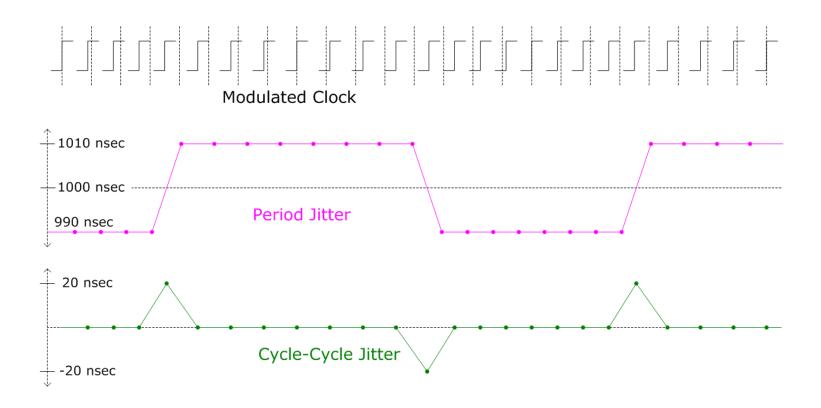
- Period Jitter
- Cycle-to-Cycle Jitter



- Cycle-to-Cycle Jitter is the first-order difference of the Period Jitter

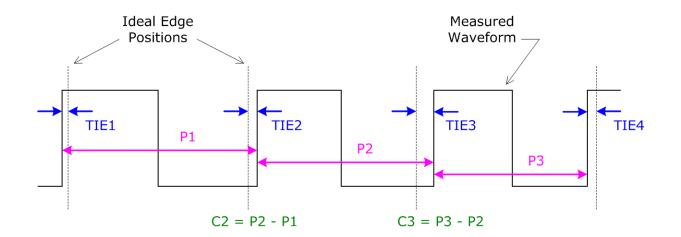


Types of Jitter (Visualization)





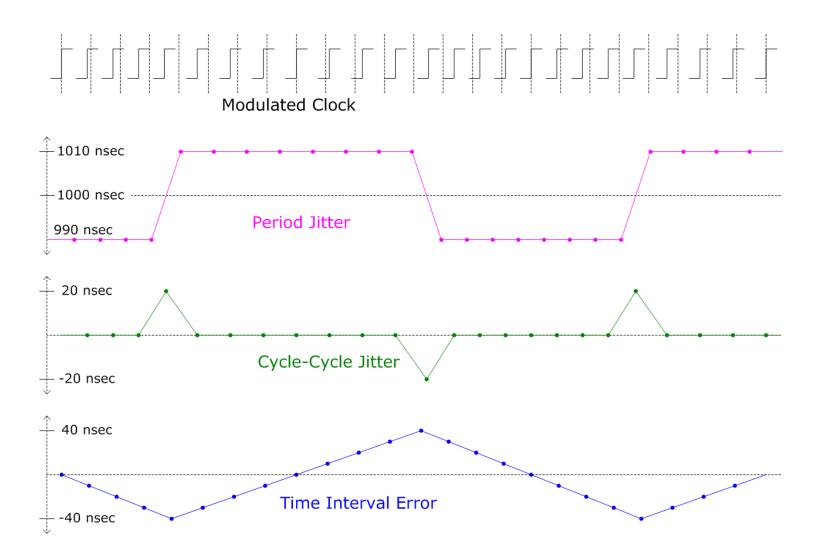
- Period Jitter
- Cycle-to-Cycle Jitter
- TIE (Time Interval Error)



- Period Jitter is the first-order difference of the TIE Jitter (plus a constant) $P_n = TIE_n - TIE_{n-1} + K$



Types of Jitter (Visualization)





Advanced Jitter - Decomposition

Rj / Dj Separation





Motivations for Jitter Decomposition

- Speed: Directly measuring error performance at 1e-12 requires directly observing MANY bits (1e14 or more). This is time consuming! Extrapolation from a smaller population can be done in seconds instead of hours.
- Knowledge: Jitter decomposition gives great insight into the root causes of eye closure and bit errors, and is therefore invaluable for analysis and debug.
- Flexibility: Already have a scope on your bench? You can do Jitter@BER measurements without acquiring more, perhaps somewhat specialized equipment.



Common Terms

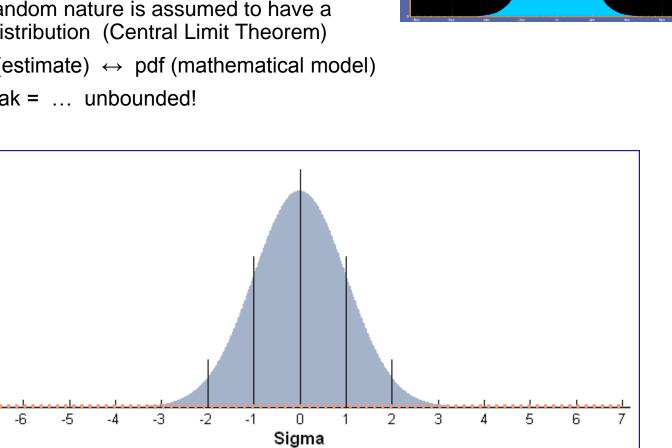
- Random Jitter (RJ)
- Deterministic Jitter (DJ)
 - Periodic Jitter (PJ)
 - Sinusoidal Jitter (SJ)
 - Duty Cycle Distortion (DCD)
 - Data-Dependent Jitter (DDJ)
 - Inter-Symbol Interference (ISI)
- Bit Error Rate (BER)
- Total Jitter ~ (TJ or TJ@BER)
- Eye Width @BER
 - versus Actual or Observed Eye Width

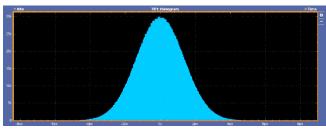




Random Jitter (RJ)

- Jitter of a random nature is assumed to have a Gaussian distribution (Central Limit Theorem)
- Histogram (estimate) ↔ pdf (mathematical model)
- Peak-to-Peak = ... unbounded!



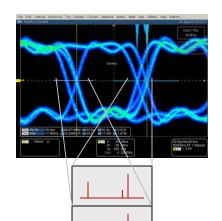


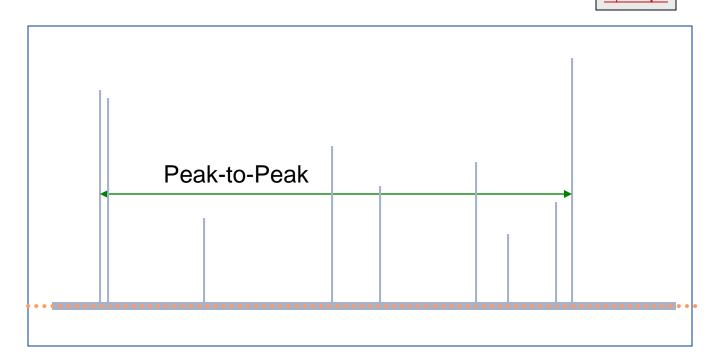
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Deterministic Jitter (DJ)

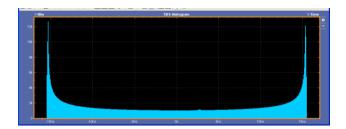
- Deterministic jitter has a bounded distribution: the observed peak-to-peak value will not grow over time
- Histogram = pdf (close enough)

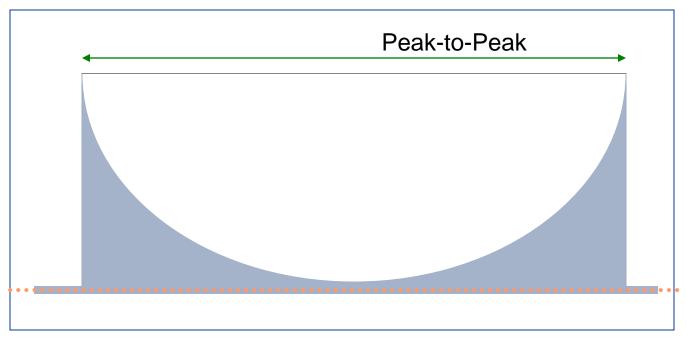




Periodic Jitter (PJ, SJ)

- TIE vs. time is a repetitive waveform
- Assumed to be uncorrelated with the data pattern (if any)
- Sinusoidal jitter is a subset of Periodic Jitter

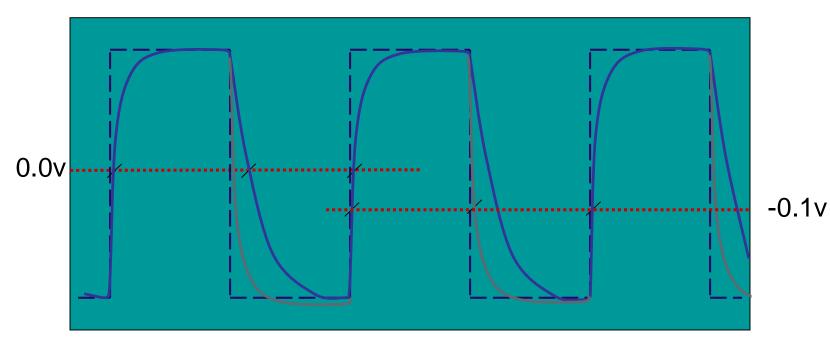


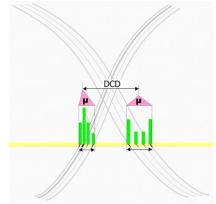




Duty Cycle Distortion (DCD)

- DCD is the difference between the mean TIE for rising edges and the mean TIE for falling edges
- Causes
 - Asymmetrical rise-time vs. fall-time
 - Non-optimal choice of decision threshold
- For a clock signal, the pdf consists of two impulses

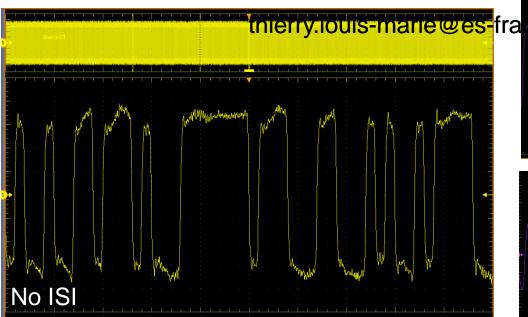


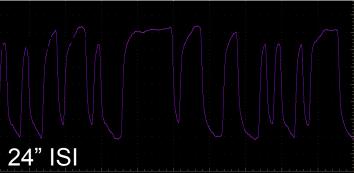


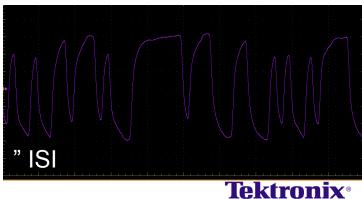
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Data-Dependent Jitter

- DDJ or PDJ used interchangeably
- ISI usually considered to be the physical effect that causes DDJ
- Characterizes how the jitter on each transition is correlated with specific patterns of prior bits
 - Due to the step response of the system
 - Due to transmission line effects (e.g. reflections)

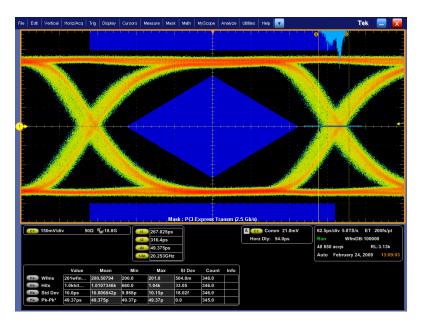




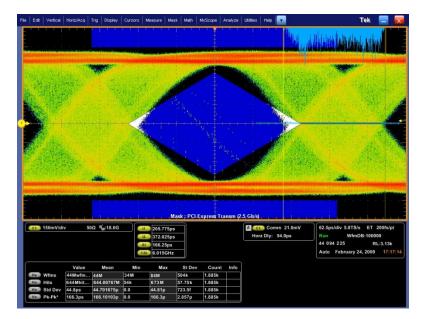


Composite Jitter Rj/Dj using dual-dirac or Spectral method?

- "Turn it on and run it for a while..."
- Historical Eye-Closure Measurement
- Jitter value including all Rj+Dj components
- Expressed as 1 sigma RMS or Pk-Pk
- Unbounded, result depends on measurement interval







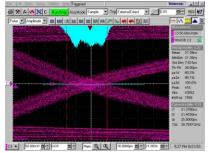
644M Hits, 44 ps RMS, 166 ps Pk-Pk

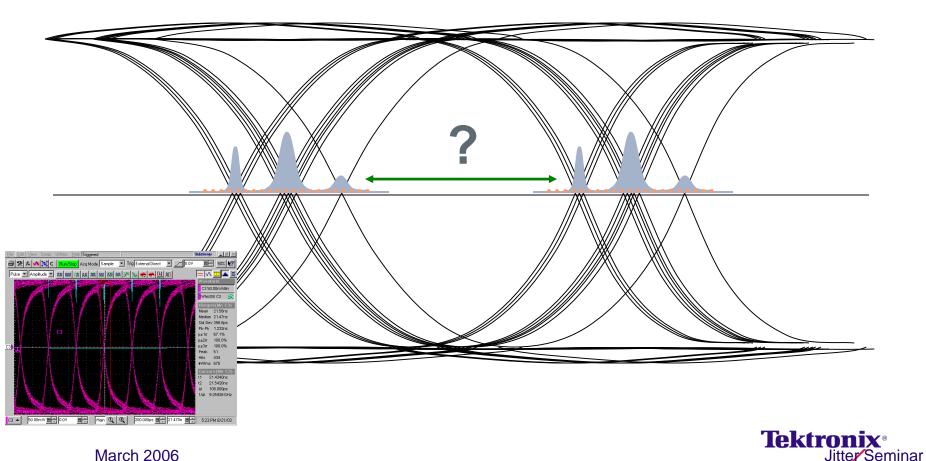


► Histograms vs. Eye Diagrams : Dual Dirac method, Rj and Dj

How open is the eye, anyway?

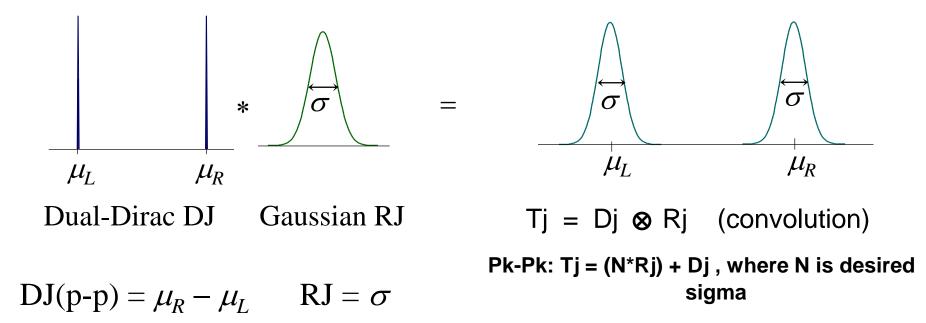
(...depends how long you watch)





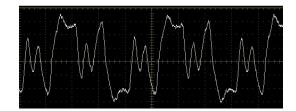
Elements of the Dual-Dirac Model

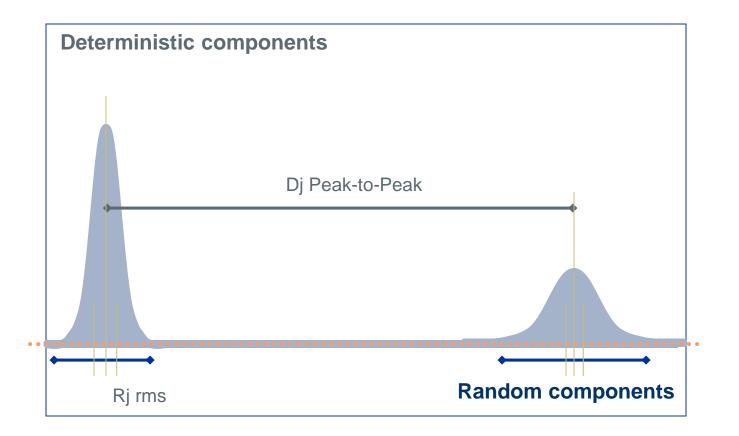
$$\left[\delta(x-\mu_L)+\delta(x-\mu_R)\right]*\frac{1}{\sqrt{2\pi\sigma}}\exp\left(-\frac{x^2}{2\sigma^2}\right)=\frac{1}{\sqrt{2\pi\sigma}}\left[\exp\left(-\frac{(x-\mu_L)^2}{2\sigma^2}\right)+\exp\left(-\frac{(x-\mu_R)^2}{2\sigma^2}\right)\right]$$



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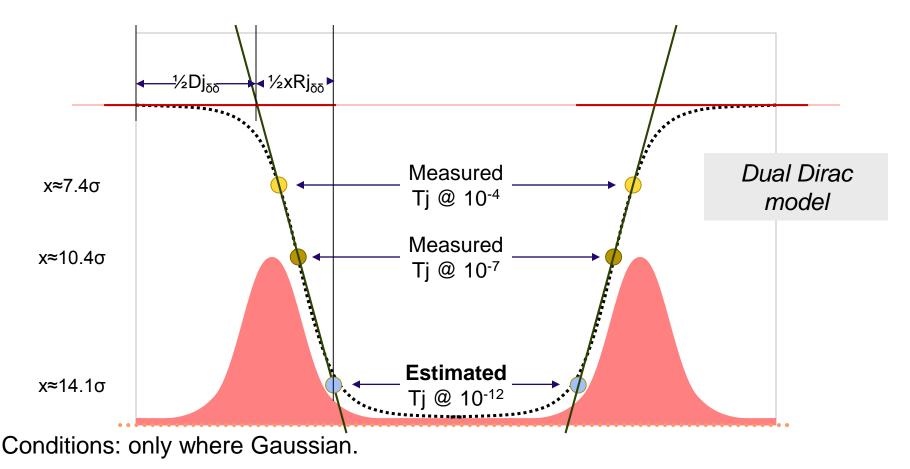


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More about Bathtub $Rj_{\delta\delta}/Dj_{\delta\delta}$ from Tj @ BER

Assume bi-modal distribution (dual-Dirac), measure Tj at two BER

Fit curve to points, slope is Rj, Intercept is Dj



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DJ(dd): Model Dependence of DJ (2)

$DJ(\delta\delta) \leq DJ(p\text{-}p)$

- ... Is the reason dual-Dirac is controversial
- It's okay for a model to have model-dependent parameters
- Make sure to use $DJ(\delta\delta)$ in $TJ(BER) = 2Q_{BER} \times RJ + DJ$

Besides

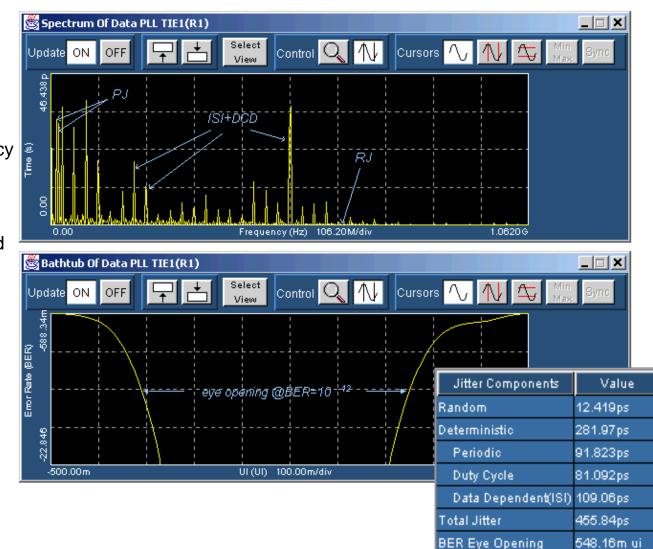
- It's easier to measure $DJ(\delta\delta)$ than DJ(p-p)
- For getting TJ(BER), $DJ(\delta\delta)$ is more useful than DJ(p-p)

BER	Q_{BER}
10-10	6.35
10-11	6.70
10-12	7.05
10-13	7.35
10-14	7.65



Spectral Method Rj/Dj but Pj DCD and ISI

- Start with
 - TIE
 - PLL TIE
- Perform FFT
 - Determine frequency and pattern rate
 - Measure RMS of background bins
 - Sum pattern related bins
 - Sum unrelated periodic bins via iFFT
 - Estimate BER



Jitter Seminar

Bounded Uncorrelated Jitter

- Interconnect and board layout technology is advancing and the greatest area of focus is in reducing the insertion loss and Signal-to-Crosstalk ratio.
- The implications of complex channel interaction can be observed and identified by examining the type and amount of Bounded Uncorrelated Jitter or BUJ.
- There is a strong Cause—and-Effect relationship between Crosstalk and BUJ which often gets classified as Random if special steps are not observed.

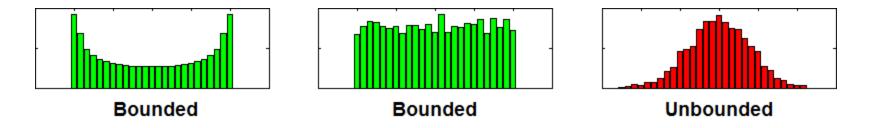
Table 4-6. Stressed Receiver Conditions

Symbol	Description
Input swing	Inner eye voltage
AC-CM_rms	AC Common Mode Voltage rms
AC-CM_pk_pk	AC Common Mode Voltage pp
BUJ	Bounded Uncorrelated Jitter
DDJ	Data Dependent Jitter
RJ	Random Jitter
נד	Total Jitter



Bounded Uncorrelated Jitter (BUJ)

- Definitions of Jitter Properties:
 - Bounded: Having a PDF (histogram) that does <u>not grow in width</u> as the observation interval increases



- Uncorrelated: Specifically, not correlated to the pattern of data bits
 - Note that PJ (Periodic Jitter) is both bounded and uncorrelated \rightarrow BUJ!
- **Deterministic**: Future behavior can be predicted based on observed past.
 - Deterministic jitter is always bounded
 - But... bounded jitter isn't necessarily deterministic
- RJ: By convention, random jitter with a Gaussian histogram
- NPJ or NP-BUJ: Non-Periodic (Bounded Uncorrelated) Jitter. This is basically random jitter with a bounded PDF



Jitter Measurement in the Presence of Crosstalk: Problem Summary

- Crosstalk-caused jitter typically is Bounded Uncorrelated Jitter (BUJ); depending on the spectra this should be separated as either
 - PJ (Periodic BUJ)

or

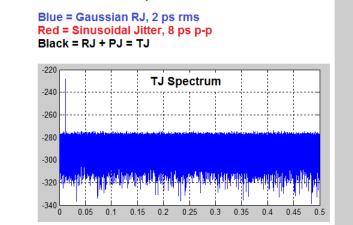
- NPJ (Non-Periodic BUJ)
- In traditional oscilloscope-based jitter measurement methodology the more spectrally diffuse BUJ components (i.e. NPJ) are not distinguished from RJ.
 - The inflated RJ is multiplied by a factor, thereby grossly inflating TJ.

Example: $TJ = DJ + 14^*RJ$ (at BER = 1e-12)

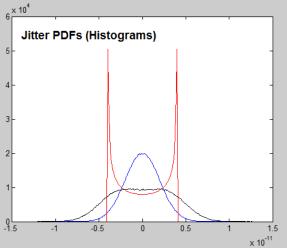
 This is well known and was documented e.g. in "Method of BER Analysis of High Speed Serial Data Transmission in Presence of Jitter and Noise", Zivny at all, DesignCon 2007.



Crosstalk Problem Summary (Graphical Version)

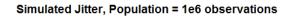


Simulated Jitter, Population = 1e6 observations



Case 1: RJ + PJ

Spectral separation works very well



RJ Spectrum

0.25 0.3

0.35 0.4 0.45

NPJ Spectrum TJ Spectrum

Blue = Gaussian RJ, 2 ps rms Red = Uniformly Distributed NPJ, 8 ps p-p Black = RJ + NPJ = TJ

-220

-240

-260 -280 -300

-320

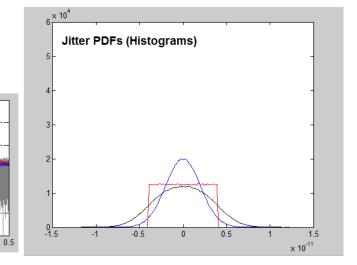
340

0.05 0.1

0.15 0.2



Spectral separation is no help at all



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Theory: Q-Scale Analysis for Detecting NPJ

 Cumulative Distribution Function (CDF) for a Gaussian Distribution:

$$CDF(x_{Gaus}) = \frac{1 + erf\left(\frac{x}{\sigma\sqrt{2}}\right)}{2}$$

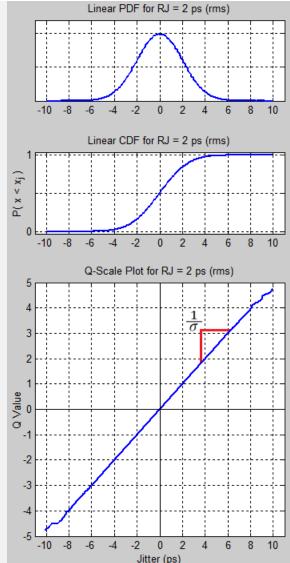
Q Scale Definition:

$$Q(x) = \sqrt{2} * erf^{-1}(2CDF(x) - 1)$$

• Q Scale for a Gaussian:

$$Q(x_{Gaus}) = \frac{x}{\sigma}$$

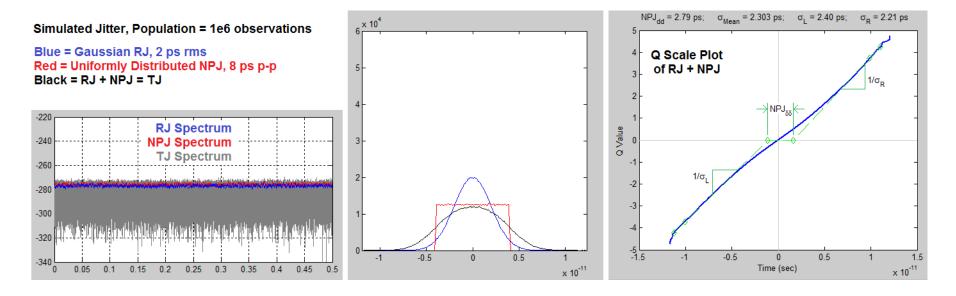
- This is a straight line with a slope of $1/\sigma!$





Separation of BUJ and RJ Jitter Components Methodology

- After PJ and DDJ are removed using the spectral approach, RJ + NPJ is converted to a histogram and then plotted using the Q Scale
- Straight lines are fitted to the left and right tails to determine both the RJ sigma and the dual-dirac weight of the NPJ



Spectral-Only Method: TJ(1e-12) = 0.00 + 3.056 * 14 = 42.8 psSpectral+BUJ Method: TJ(1e-12) = 2.79 + 2.303 * 14 = 35.0 ps



DPOJET Setup for BUJ / NPJ Measurements

- Enable Spectral+BUJ either through the Preferences Setup or the Jitter Map
- Minimum # of UI control is only available via Preferences Setup
 - Default is 1M but it can be reduced as low as 10k.
 - Agilent EZJIT has a similar (non-adjustable) population requirement, ~ 150k

Preferences S General	Dual Dirac Model	PCI/FB-DIMM	
Measurement	Jitter Separation Model	Spectral Only	
Jitter Decomp		2°	
Path Defaults		Preferences Setup	
		General Dual Dirac Model PCI/FB-DIMM V	
		Measurement Jitter Separation Model Spectral + BUJ V	
		Jitter Decomp Minimum # of UI for BUJ Analysis 1M	
		Path Defaults	
		OK Car	



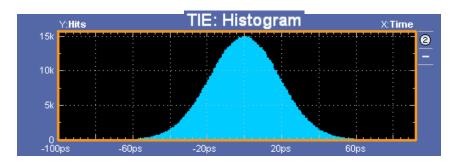
DPOJET Results for BUJ / NPJ Measurements

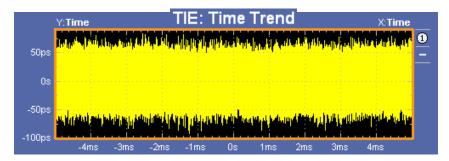
 Clock NPJ measurement shows actual progress toward the population requirement

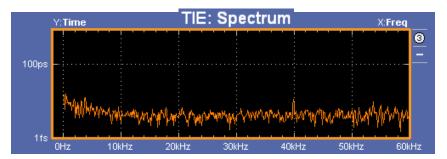
Select					View Details T Expand			Recalc		
	L Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc	0
Configure	🕨 🗉 TIE1, Ref1	1.8264fs	6.4070ps	21.080ps	-19.748ps	10.828ps	392399	23.295ps	-22.010ps	
connigure	🛨 TJ@BER1, Ref1	< Min #of UI		5% complete			0			Single
	🛨 RJ1, Ref1	< Min #of UI		5% complete			0			
Results	🛨 Clock NPJ1, Ref1	< Min #of UI		5% complete			88070			Run
	🛨 PJ1, Ref1	12.868ps	0.0000s	12.868ps	12.868ps	0.0000s	1	0.0000s	0.0000s	
Plots	🛨 DDJ1, Ref1	18.375ps	0.0000s	18.375ps	18.375ps	0.0000s	1	0.0000s	0.0000s	Show Plots
	🕣 DCD1, Ref1	1.0108ps	0.0000s	1.0108ps	1.0108ps	0.0000s	1	0.0000s	0.0000s	ulli



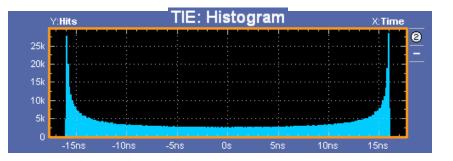
Jitter Visualization

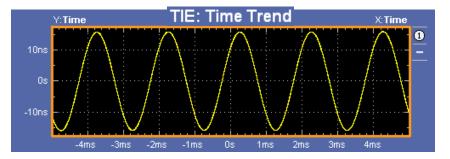


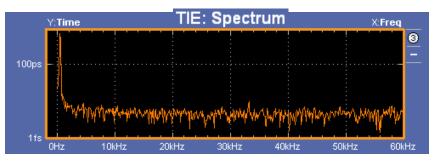




Gaussian Random Noise





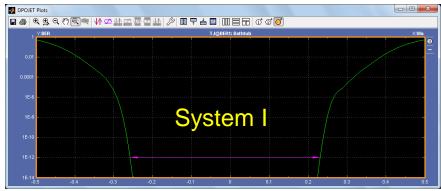


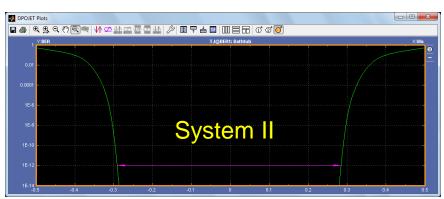
Sinusoidal Jitter

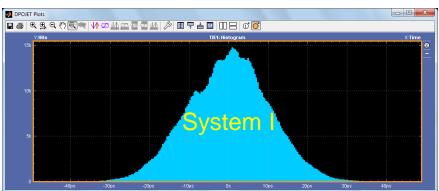


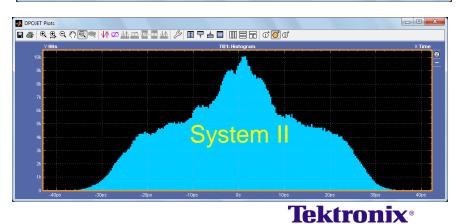
Jitter Visualization – Bathtub Plot

- Shows the Eye Opening at a Specified BER Level
- Note the eye closure of System I vs. System II due to the RJ- RJ is unbounded so the closure increases as BER level increases
 - System I has .053UI of RJ with no PJ
 - System II has .018UI of RJ and .14UI of PJ @ 5 and 10Mhz



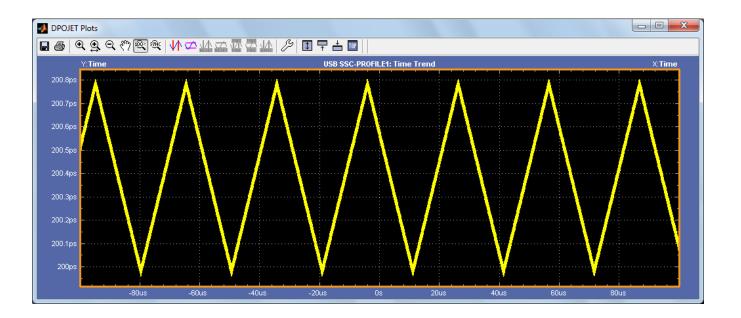






Jitter Visualization – Time Trend

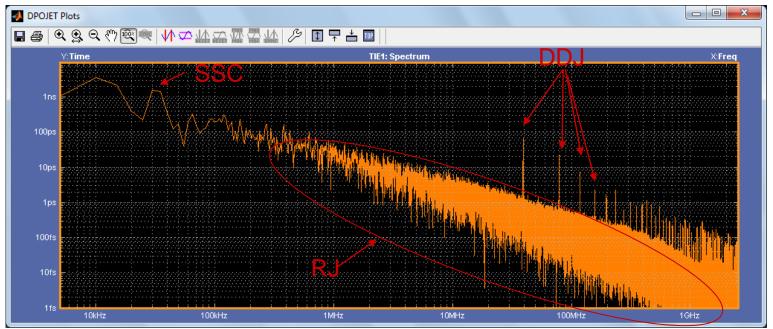
- Histogram does not have any context of time
- Time Trend can reveal repeating patterns that may indicate modulation on the signal
 - For example 5 cycle of SSC @ 30khz as shown below





Jitter Visualization – Spectral Plot

- Frequency domain view of the signal content
- Deterministic components show as lines above the noise
 - DDJ is at frequencies of the bit rate / pattern length (example below is 5Gb/s PRBS7) Note the spikes at intervals of 40Mhz in the plot.
 - Constant Clock CR was used





TIE Jitter needs a Reference Clock

- The process of identifying the reference clock is called **Clock Recovery**.
- There are several ways to define the reference clock:
 - Constant Clock with Minimum Mean Squared Error
 - This is the mathematically "ideal" clock
 - But, only applicable when post-processing a finite-length waveform
 - Best for showing very-low-frequency effects
 - Also shows very-low-frequency effects of scope's timebase
 - Phase Locked Loop (e.g. Golden PLL)
 - Tracks low-frequency jitter (e.g. clock drift)
 - Models "real world" clock recovery circuits very well
 - Explicit Clock
 - The clock is not recovered, but is directly probed
 - Explicit Clock (Subrate)
 - The clock is directly probed, but must be multiplied up by some integral factor

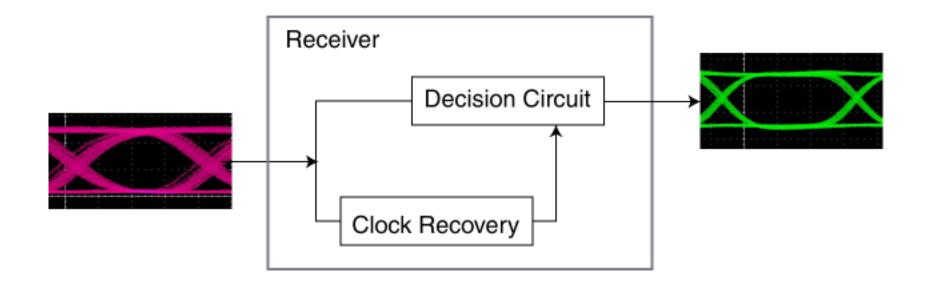


Reference Clock for Jitter : Clock Recovery?

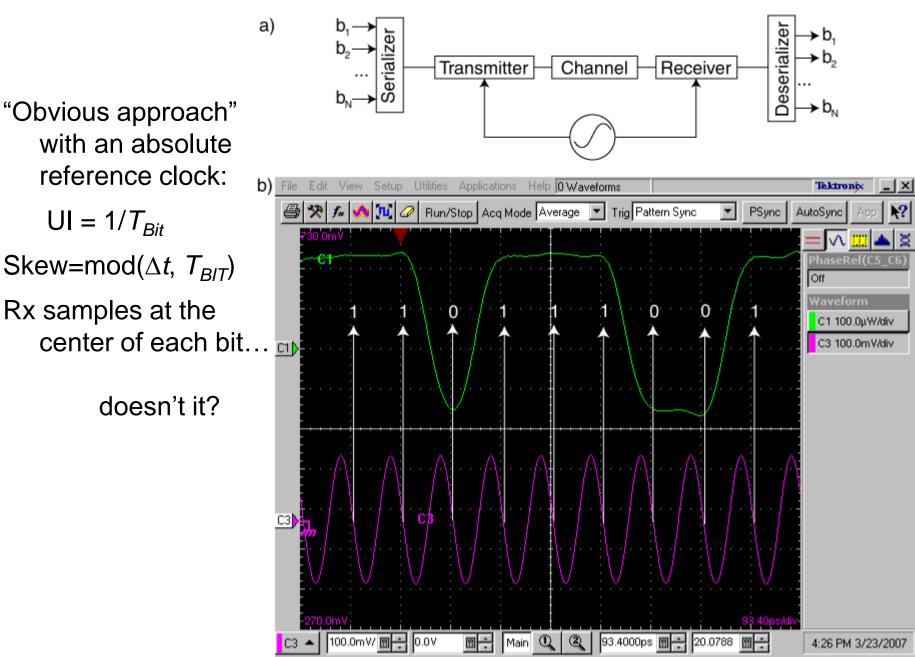
In a receiver

- The clock positions the sampling point
- Comparator determines logic level

How can we reduce the effect of jitter in the decision circuit?

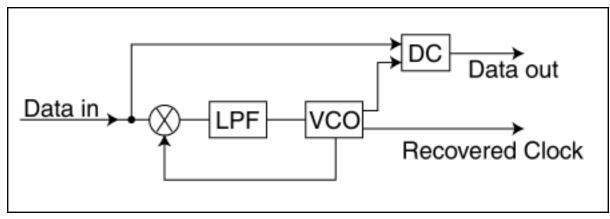


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Phase Locked Loop Clock Recovery



To extract a useful clock, the data must...

- Have plenty of logic transitions
 - No long runs of identical bits
- Be DC balanced

Data signals are encoded, e.g., 8B/10B encoding

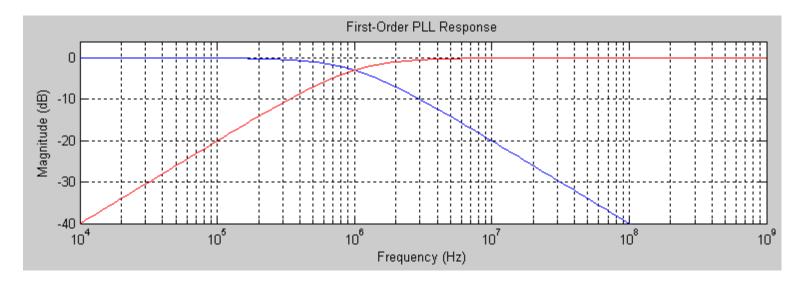


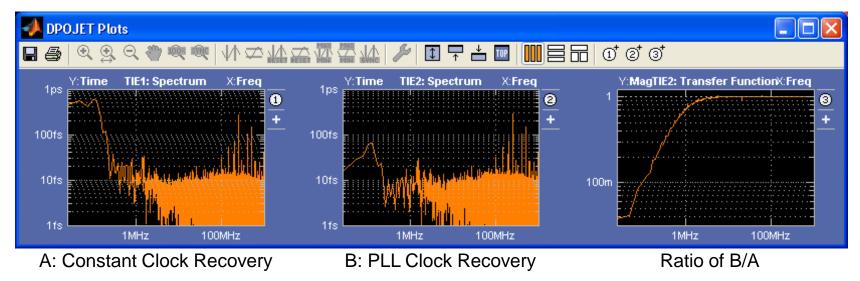
JTF vs PLL Loop Bandwidth

- Configuring the correct PLL settings is key to correct measurements
- Most standards have a reference/defined CR setup
 For example, USB 3.0 uses a Type II with JTF of 4.9Mhz
- Type I PLL
 - Type I PLL has 20dB of roll off per decade
 - JTF and PLL Loop Bandwidth are Equal
- Type 2 PLL
 - Type II PLL has 40dB of roll off per decade
 - JTF and PLL Loop Bandwidth are not Equal
 - For example, USB 3.0 uses a Type 2 PLL with a JTF of 4.9Mhz. The corresponding loop bandwidth is 10.126 Mhz
 - Setting the Loop Bandwidth as opposed to JTF will lead to incorrect jitter measurement results



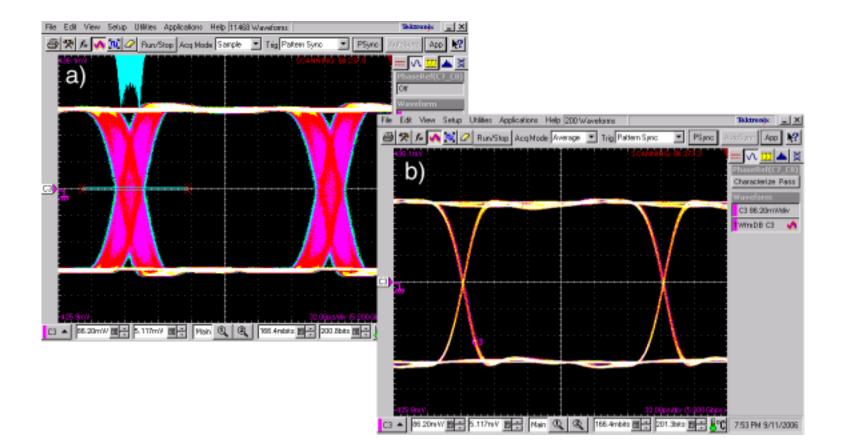
PLL Loop Bandwidth vs. Jitter Transfer Function (JTF)







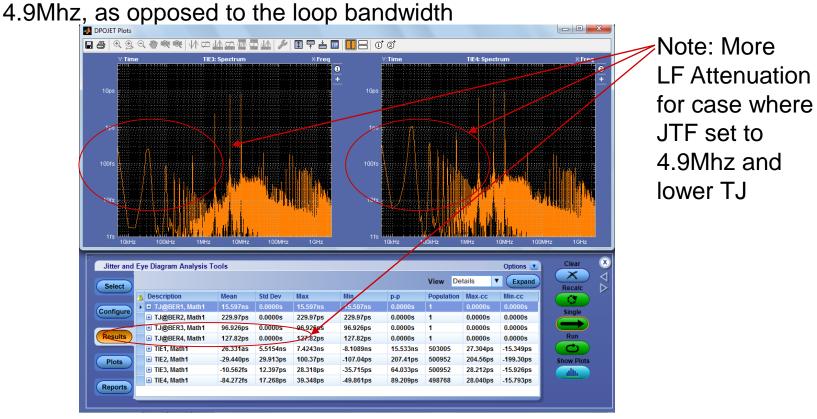
Effect of CR Bandwidth on Eye Opening





Results depend on CR Settings USB 3.0 Example

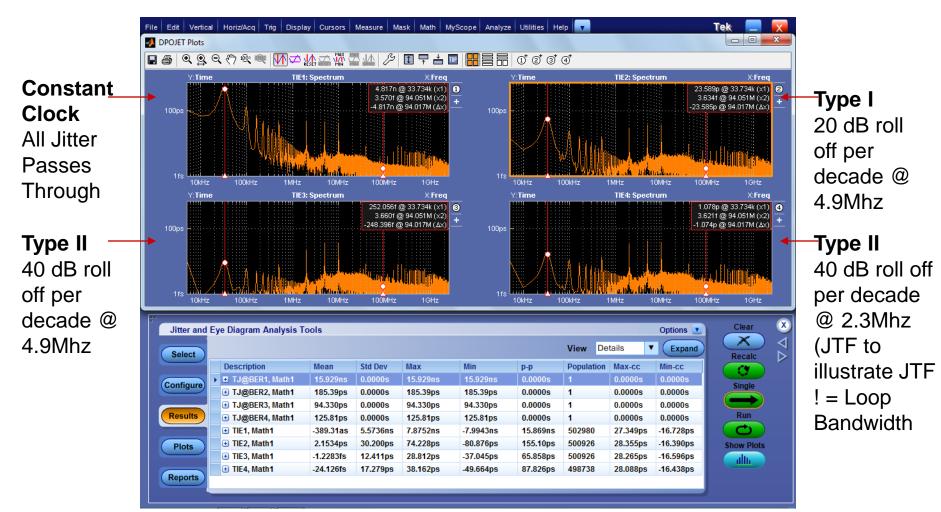
- The example below shows the effects of using a JTF set to 4.9Mhz vs. Loop Bandwidth set to 4.9Mhz for a Type II PLL
- Note the difference in the jitter that is tracked
 - The results on the left are correct as the JTF was properly set to



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Further Comparison of PLL Types using Spectrum Plots

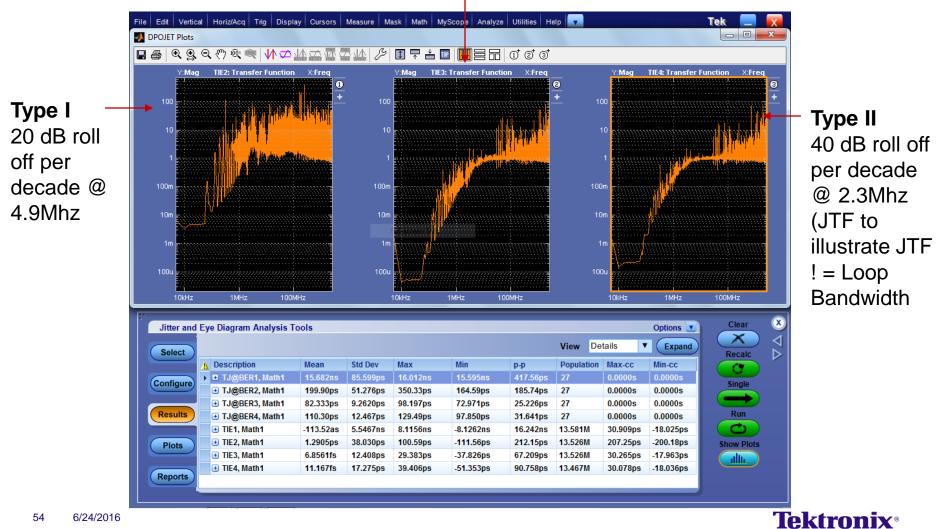


First Cursor in each plot is @ 33Khz to illustrate effect on SSC

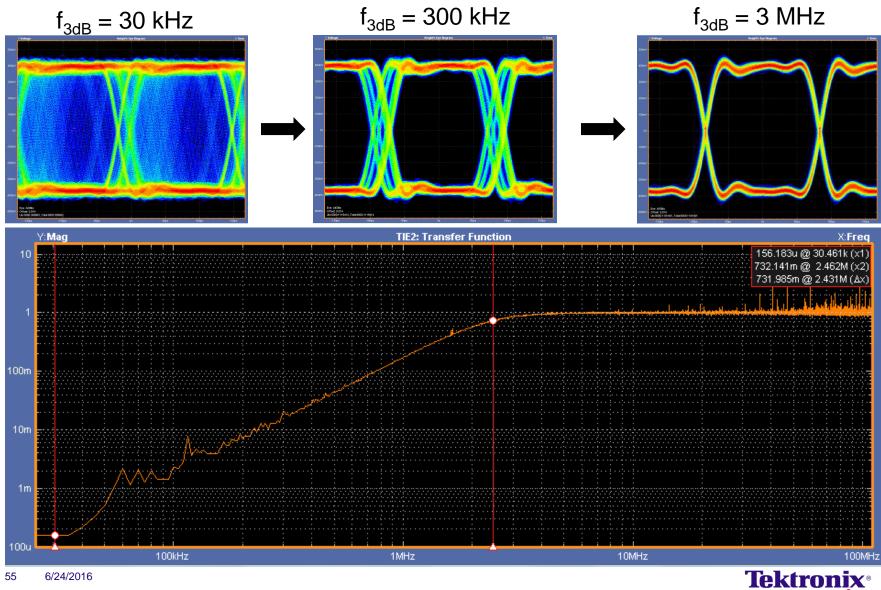


Further Comparison of PLL Types using Transfer **Function Plots**

Type II 40 dB roll off per decade @ 4.9Mhz

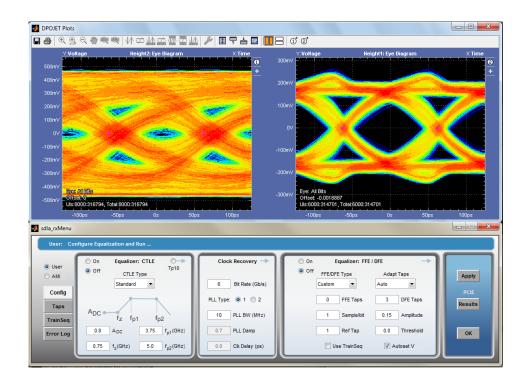


JTF Filtering Effects based on different PLL bandwidths



Open Closed Eyes Apply Receiver Equalization

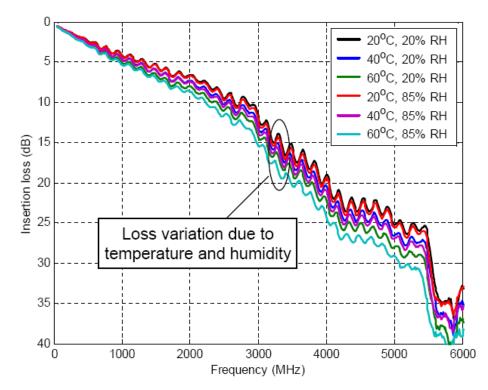
- The example below shows a PCI Express 3.0 signal at the far end (input to the receiver)
 - Note that the eye is closed
 - Note that clock recovery would have failed due to the channel loss
 - After applying DFE equalization the signal can be measured with DPOJET





The problem is the channel ...

 \rightarrow Channel exhibits large frequency dependent loss

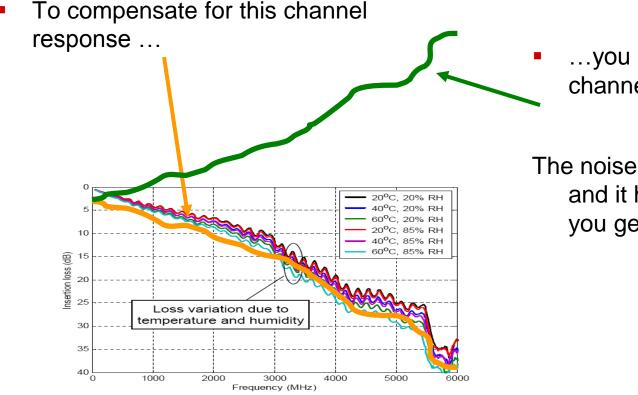


- Loss/dispersion of the channel closes the eye
- Receivers now incorporate methods to compensate for loss (equalization)

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Equalization: The solution #1: High Frequency "Boost"

The problem is just what you'd think it would be:

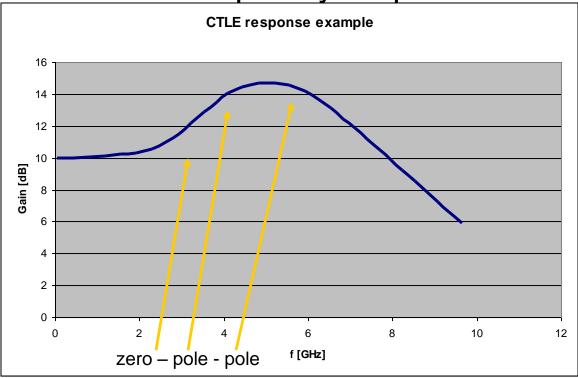


...you need to boost the channel so much.

The noise amplification is huge, and it hurts the improvement you get (Signal to noise)



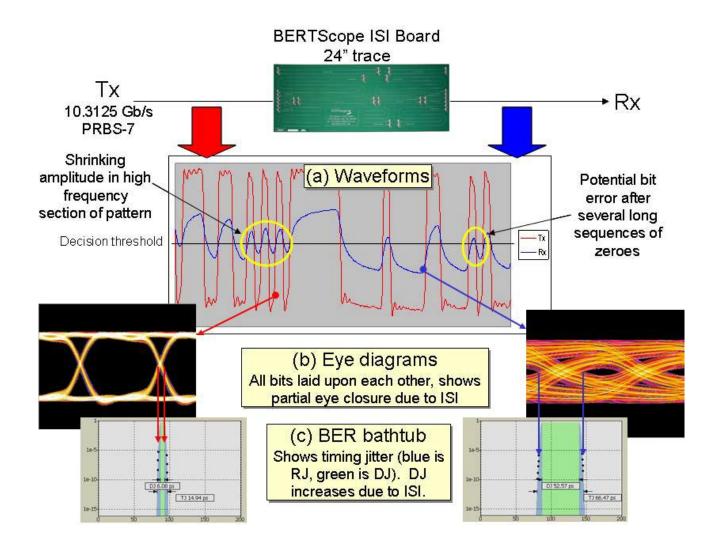
Equalization: CTLE frequency response



- CTLE Continuous Time Linear Equalization
- Linear HF filter/boost
- Advantages: Low power & Simple implementation
- ... but it amplifies noise

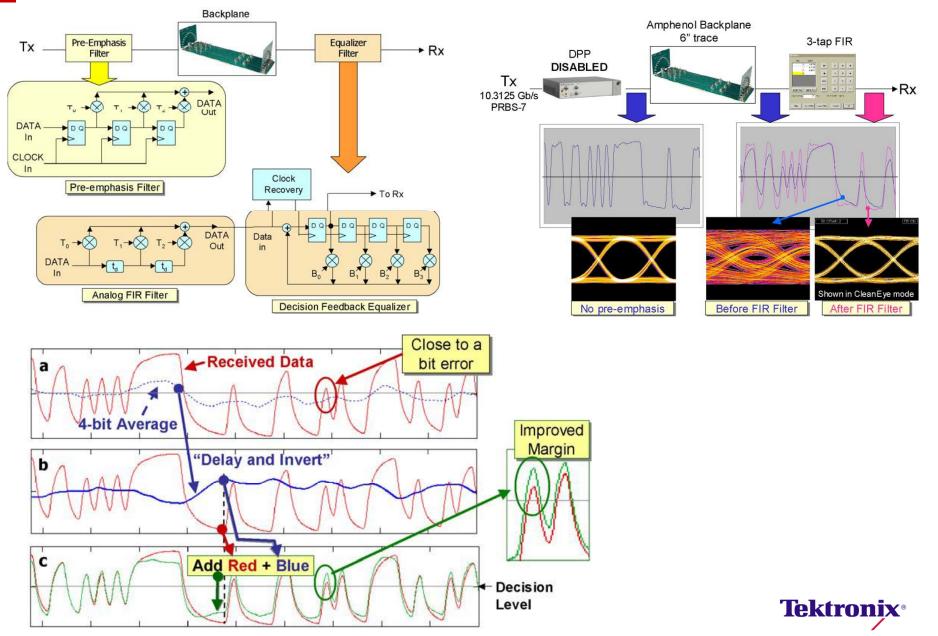


Channel Testing Simulate Compliance Channels





Channel Testing Simulate Compliance Channels

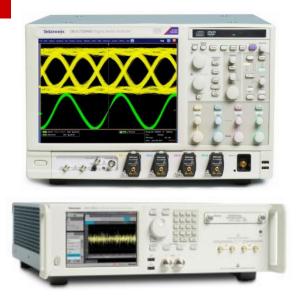


Trois Instruments pour la même mesure Tx?





Real-time Scope, Sampling Scope, BERT Scope







Scope BW 70GHz AWG BW 18GHz

Standard tool for Tx test Datacom

Rx test < 6.25Gbits

Optical and Electrical BW 80GHz

Standard tool for Tx test Telecom

No Rx test

BERT Scope 28.6Gbits Tx/Rx

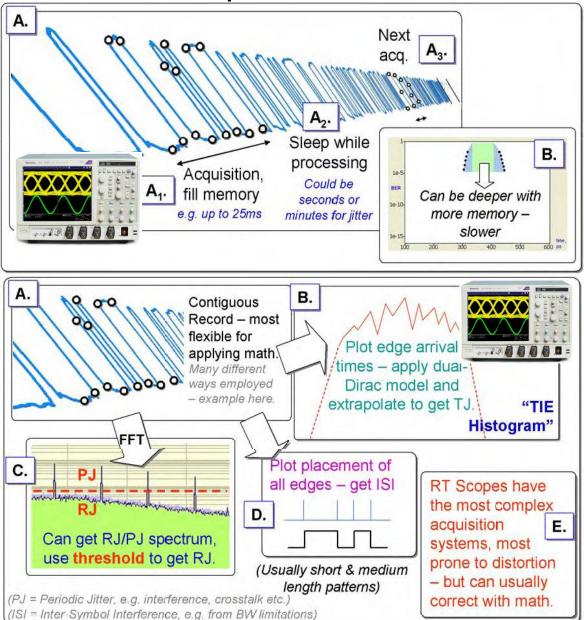
PPG 40Gbits Tx/Rx

Standard tool for Rx test Super High speed

No Tx test



Real-time Scope



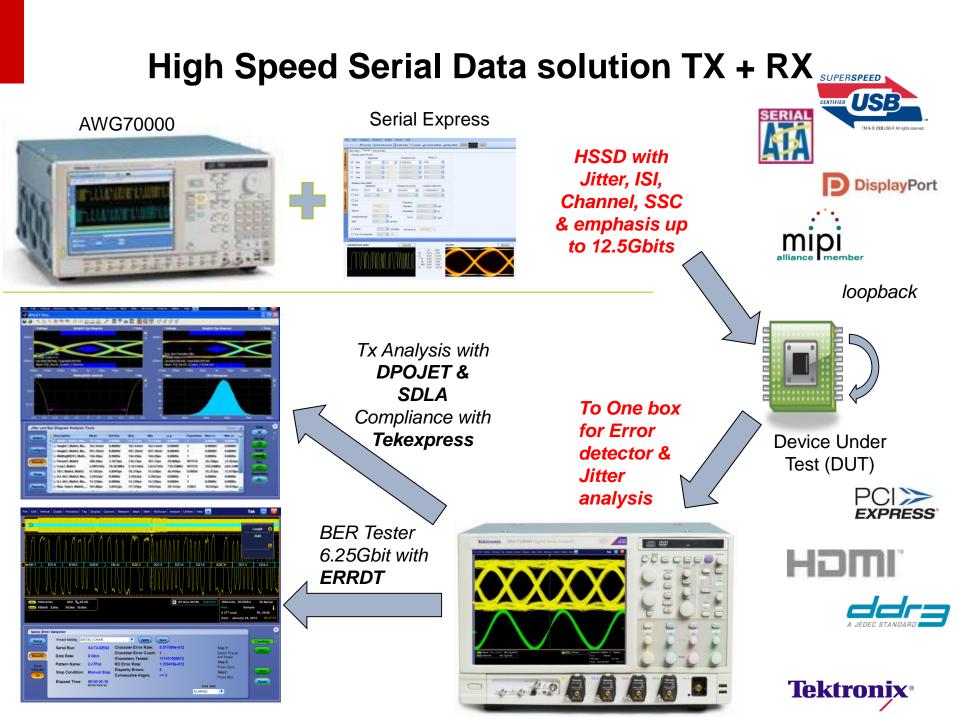
Advanced trigger on signal No clock need

Built in Clock recovery

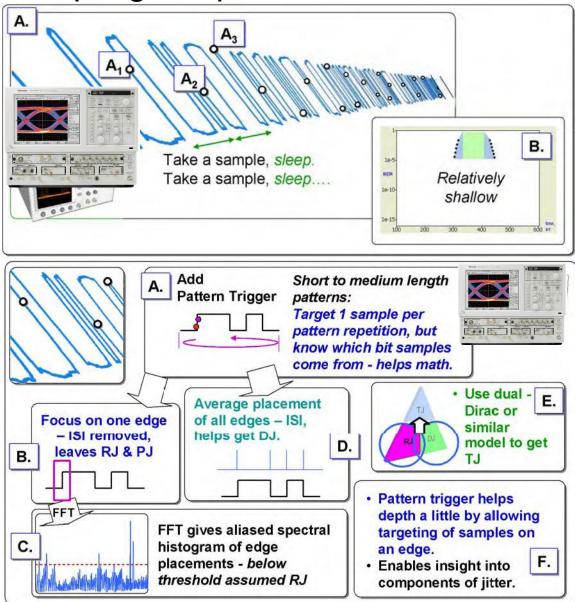
One sample every 5ps with continue acquisition (depend on memory)

Dual-Dirac /spectral and Q-scale method for complete Tx analysis

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Sampling Scope



Electrical and Optical acquisition

Need external trigger clock

Need external Clock recovery

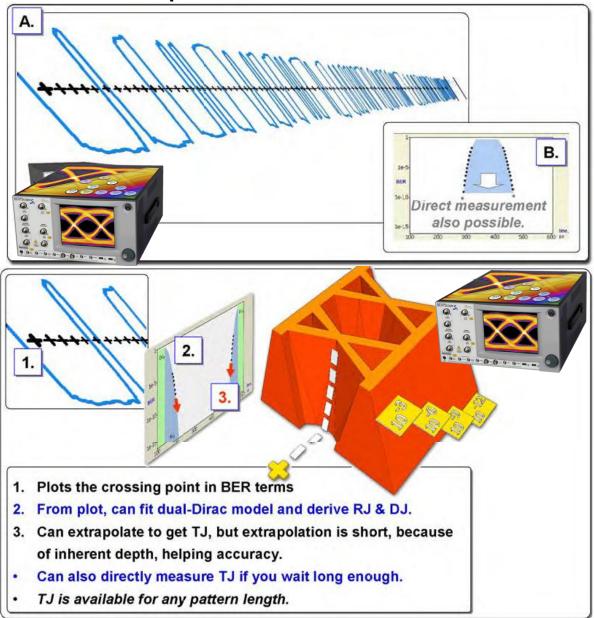
Only Tx measurement

80GHz BW but only repetitive acquisition at 300kS/s

Very precise Rj measurement. Trigger Jitter scope <100fs

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BERT Scope



Need external trigger clock

Need external Clock recovery

28.6Gbit Rx and Tx

See all bit and can measure Tj directly (no extrapolation)

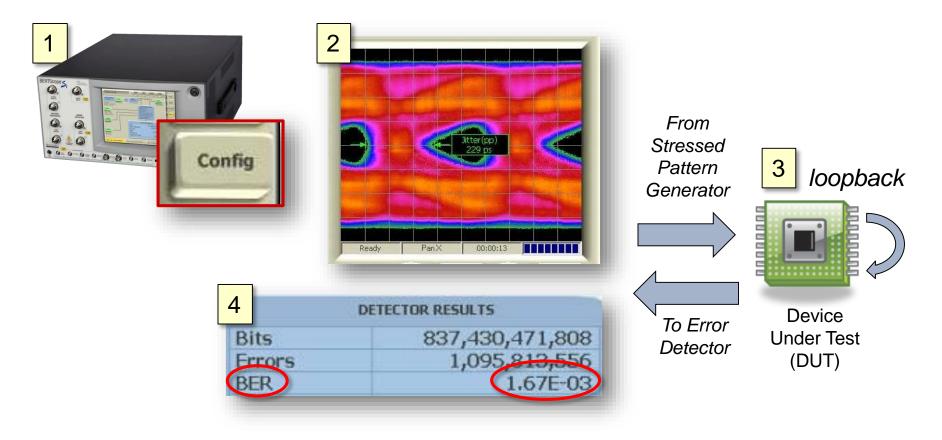
Stressed Eye capability

Eye diagram and Jitter map capability

Error Location capability

PRBS31 length capability Tektronix®

1. Stressed Receiver Tolerance Testing Start Testing Quickly

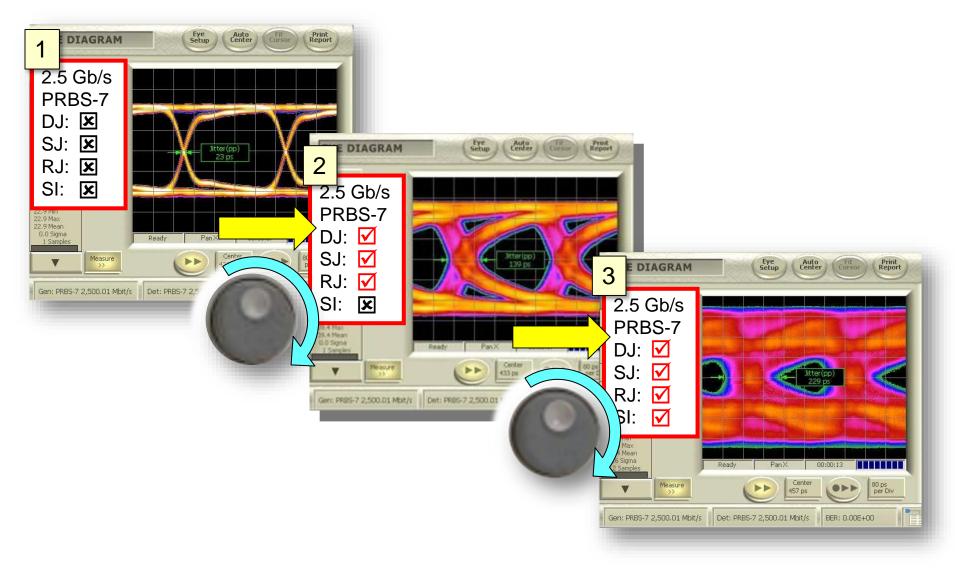


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- 1. Recall stressed eye configuration
- 2. Apply stressed eye signal to DUT's receiver
- 3. DUT loops received bits back to BERTScope Error Detector
- 4. BERTScope counts any errors

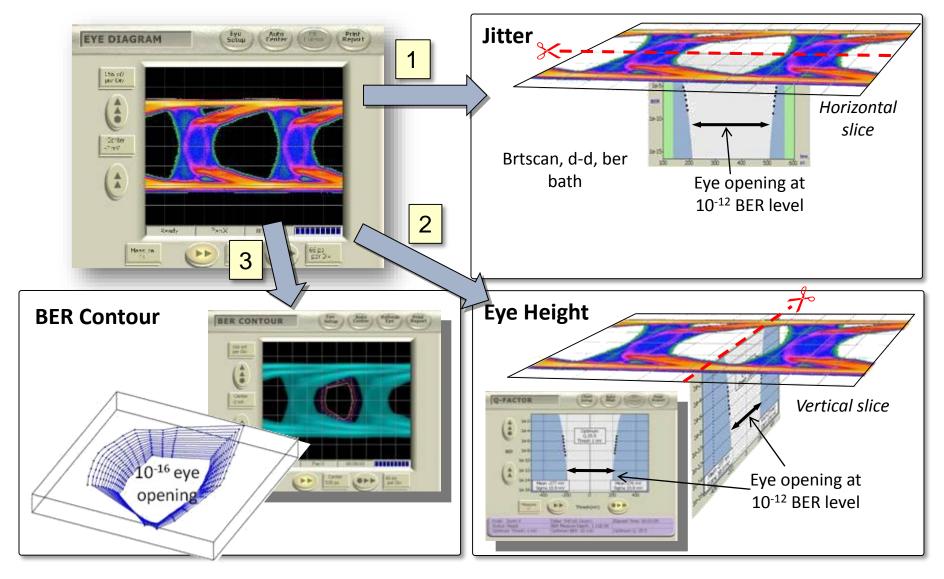
2. Creating the Stressed Signal

Dynamically change Data Rate, Stress, Pattern



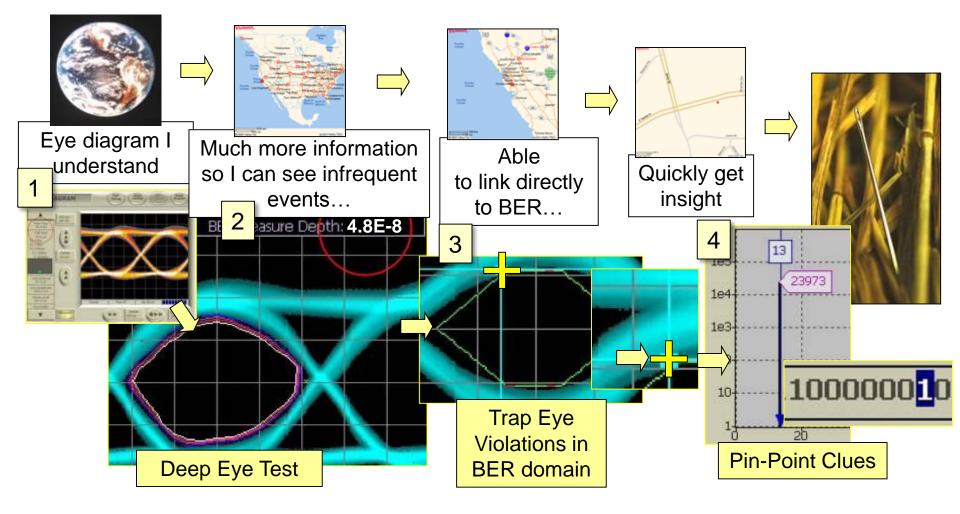
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3. BER-Based Analysis Deep Insight with the BERTScope Toolkit



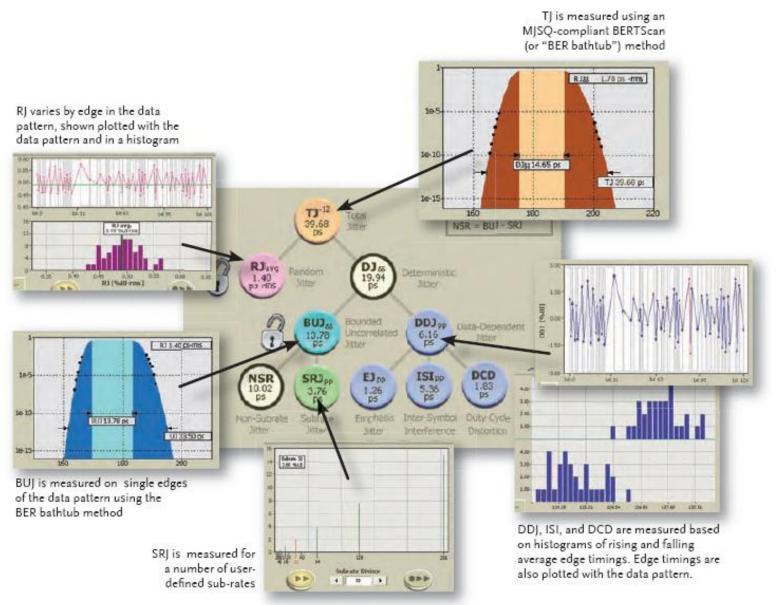


4. Drilling Down From Eye to Errors Linked Tools Enable Deep Insight



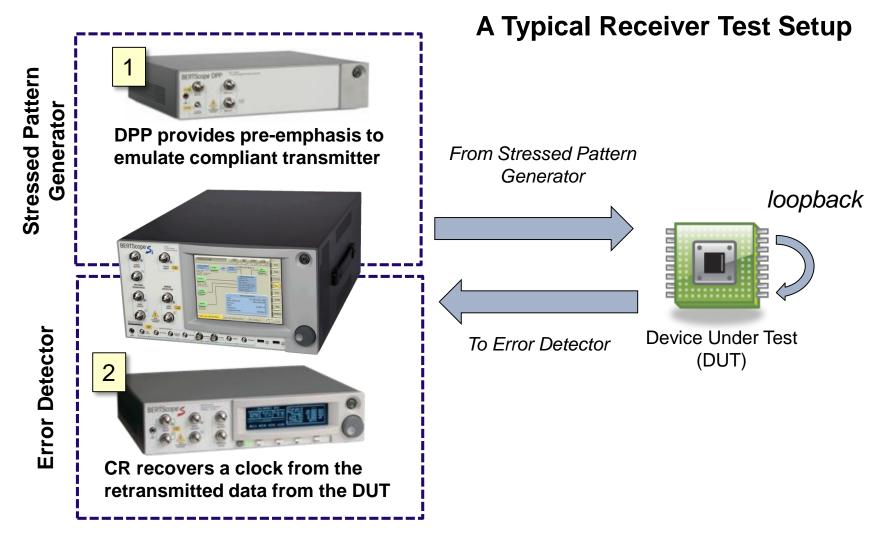


5. Jitter Map





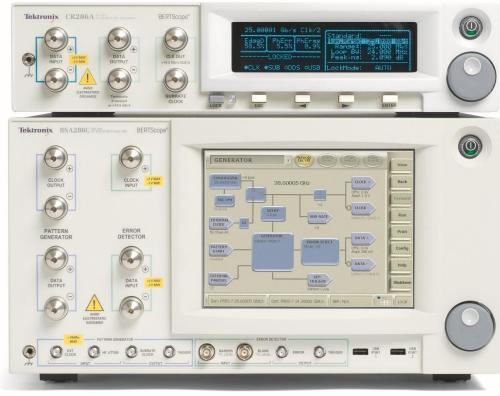
6. The Right Companion Products The BERTScope Product Family Makes Compliance Easy

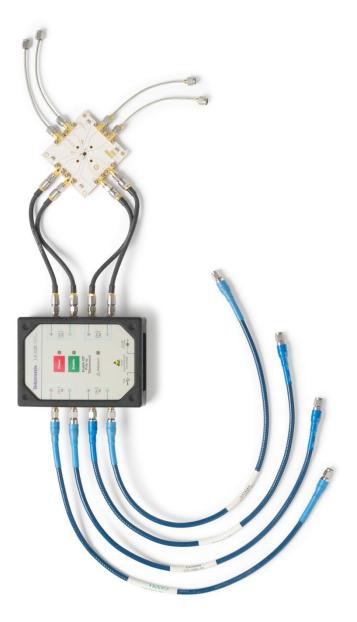


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BERTScope® Family of Products

 BSA Family is a series of BERT and Analysis tools spanning 500Mbps to 28.6Gbps. Upgrades avenues from lower performing units to higher performing ones will continue to be preserved.







Tektronix LE320/LE160 32 & 16Gbps Linear Equalizer Product Introduction

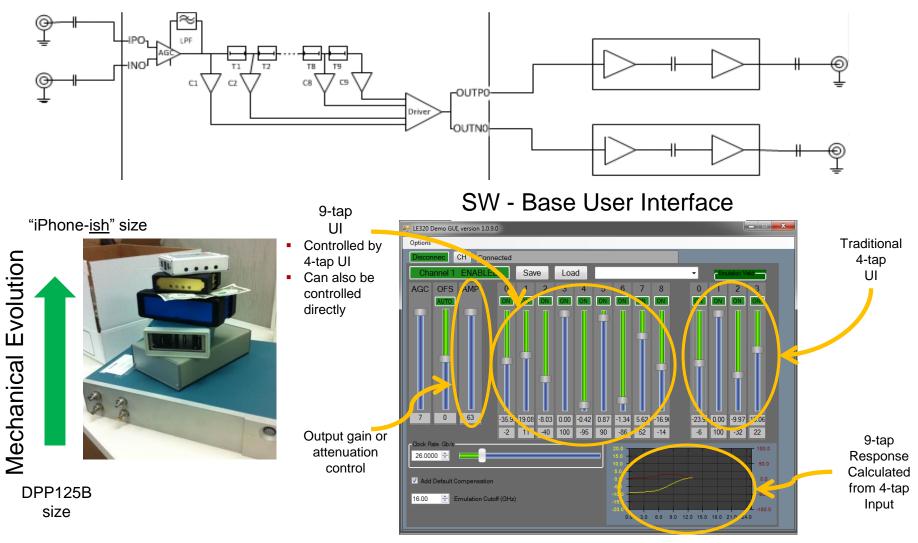
- Compact two channel 32Gbps 9
 Tap linear equalizer design in a "remote module" configuration
- +-20dB tap controls offer flexible pre-emphais or channel de-embed capabilities.
- User (and PI) configurable filter properties allows flexible parametric equalization
- Electronically switchable frequency dependent filter capability permits DDJ tolerance testing and testing against known reference channel models
- Front-end signal path (CTLE) for Sampling or BERT Instruments





Tektronix LE320 32G Linear Programmable Equalizer

9 Tap linear equalizer design, supporting 14-32Gbps operation



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PPG/PED

PPG Base Instruments

- **PPG1251** 12.5Gb/s PPG
 Jitter insertion (LF+HF)
- PPG300X 30Gb/s PPG
 1/2/4 Channel
 LF jitter insertion
 - HF jitter insertion

- PPG320X 32Gb/s PPG

- 1/2/4 Channel
- Adjustable output
- LF jitter insertion
- HF jitter insertion
- PPG4001 40Gb/s PPG
 - LF jitter insertion
 - HF jitter insertion



PPG3204 32Gb/s 4 channel PPG



PED3202 32Gb/s 2 channel PED

PED Base Instruments

- PED320X 32Gb/s PED
- —— 1/2 Channel
- —— Full or half rate clock input
- —— AC or DC coupled input

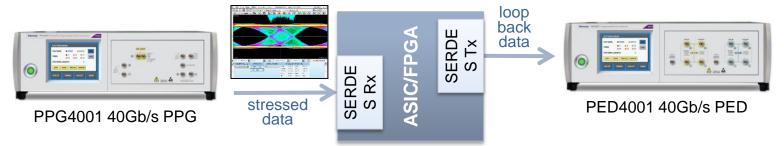
- PPG400X 40Gb/s PED

- 1/2 Channel
 - —— Full or half rate clock input
 - AC or DC coupled input



32Gb/s and 40Gb/s SERDES JTOL testing

SERDES JTOL Testing



Some ASICs/FPGAs have built-in BER testing and don't require loop back with a PED

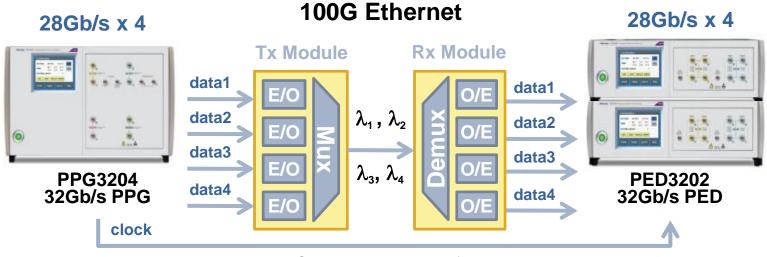


Advantages

- Separate PPG and PED for users with on-chip BER capabilities
- Low intrinsic jitter
- Fast rise-fall times and high signal integrity
- SJ/RJ/BUJ insertion for standards compliance tests
- Software analysis tools (bathtubs, JTOL, J2/J9, etc)
- Easy-to-use touchscreen and USB programmability



100G Ethernet SR4/LR4/ER4 transceiver testing



Note: Tektronix CR286 may be added for clock recovery



Advantages

- Flexible multi-channel solution
- Low intrinsic jitter
- · Fast rise-fall times and high signal integrity
- SJ/RJ/BUJ insertion for standards compliance tests
- Software analysis tools (bathtubs, JTOL, J2/J9, etc)
- Easy-to-use touchscreen and USB programmability

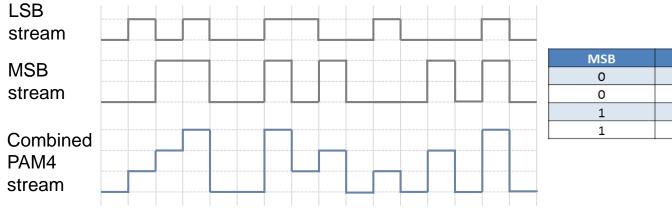


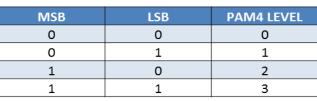
What is PAM?

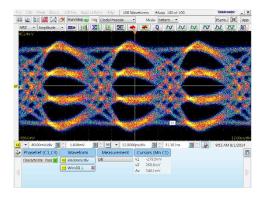
Pulse Amplitude Modulation

-PAM4 combines two bit streams and uses 4 levels to encode 2 bits into 1 UI

-For Example, 56 Gbit/s PAM4 runs at a symbol rate of 28 GBaud







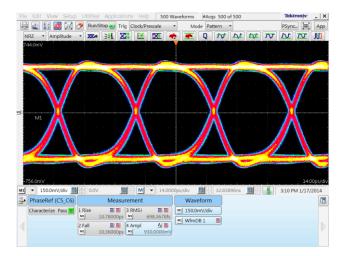


What are the differences between PAM4 and NRZ?

- PAM4
 - 4 Levels \rightarrow 3 Eyes
 - Sensitive to SNR (eyes smaller)
 - 2 bits into 1 UI
 - ½ Symbol Rate for same data throughput (28 GBaud = 56Gbps)
 - Adds complexity/cost to Tx/Rx
 - Image: New York
 Verify Series
 Image: New York
 Node
 Part 100 d100
 Takramity
 X

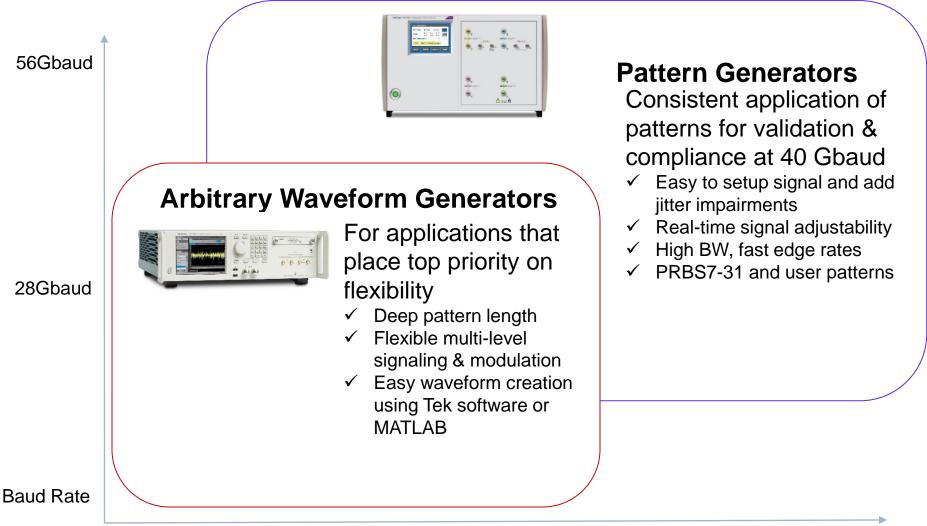
 Image: New York
 PunkSope
 Trig
 Clock/Presale
 Mode
 Part
 Applications
 Part
 Part

- NRZ
 - − 2 Levels \rightarrow 1 Eye
 - Less Sensitive to SNR
 - 1 bit in 1 UI
 - 2X Symbol Rate for same data throughput (28GBaud = 28Gbps)





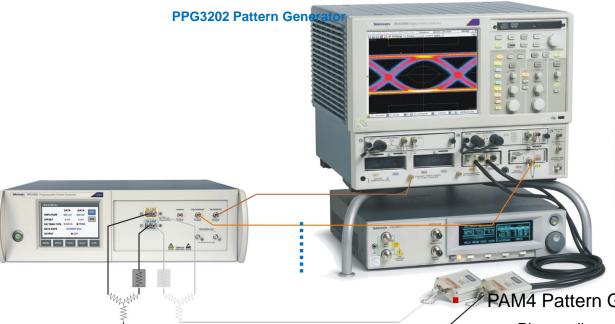
Considerations for a PAM4 Signal Generation Engine



Manufacturing



PAM4 Generation & BER Analysis using Pattern Generators





- PED3202 Error Detector
- BERT products bundled into a PAM4 system:
 - Programmable pattern generator
 - Programmable error detector
 - Analysis software
 - **Broadband components** (power combiners/attenuators)

- PAM4 Pattern Generator
 - Phase-aligned channels simplify multi-level signal generation
- User-programmable data patterns allow test of PAM4 custom data
- PAM4 Error Detector
 - BER measurements analyzes every bit of each pattern
 - Contour plots, bathtub curves, total jitter analysis via software tools
 - Can be used for BER measurements generated by PPG and/or AWG



Test Methodologies for PAM Signaling Validation

Tektronix provides complete support for validation of PAM4 at 28 & 56G

